# A versatile phase shifter for NMR experiments and other applications

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# A versatile phase shifter for NMR experiments and other applications

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**Abstract.** It is impossible to construct an ideal phase shifter, one whose phase shift and gain is independent of frequency, using a linear circuit. The reasons for this are discussed and the compromises necessary in some practical implementations are examined. Following this, a novel circuit using programmable delay lines is presented. Such circuits have proved particularly useful in NMR systems.

## 1. Introduction

Many areas of electronic instrumentation require the use of phase shifters. Accurate, stable and reproducible shifts of variable angle are often required. At first sight it is somewhat surprising that each different application seems to have its own phase shift implementation; there is no simple standard/universal method. Considering an idealized phase shifter, constructed as a self-contained instrument, it is easy to specify its required characteristics. The output would be shifted in phase from the input by a specified, adjustable angle while its magnitude would be equal to that of the input. In particular these features would, for an instrument of general application, be independent of the frequency of the input signal. By the very language used this is what would happen to sinusoidal signals; the effect on other waveforms would, in a linear circuit, be determined by Fourier superposition.

## 2. Linear circuit implementations

Unfortunately, it is impossible to realize the ideal behaviour of phase shift and amplification independent of frequency in any circuit operating in a linear fashion. It would involve a violation of the principle of causality, as realized by Bode (1940). More familiarly, the in-phase and the quadrature component of a realistic transfer function are not independent; they are connected by a pair of Kramers–Kronig relations. Thus differentiators and integrators provide a frequency-independent phase shift of $\pm 90°$ but the output signal magnitudes are respectively proportional to and inversely proportional to frequency; the first requirement is satisfied but not the second.

Conversely the output of the RC network shown in figure 1 has a frequency-independent magnitude since

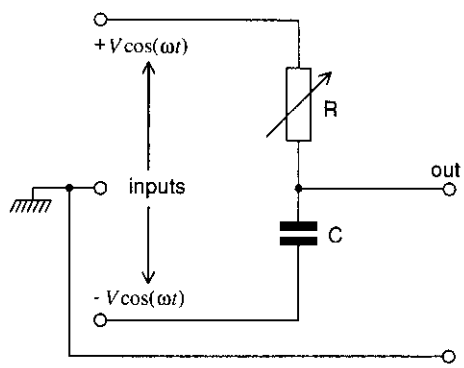


**Figure 1.** Analogue network for producing phase shifts at constant amplitude.

the transfer function is $(1-j\omega RC)/(1+j\omega RC)$ whose modulus is unity, but the phase angle varies with frequency through $\phi = \tanh\{2\omega RC/(1-\omega^2R^2C^2)\}$. The second requirement is satisfied but not the first.

Delay lines also fall into this second category. The invariant quantity is the time delay. The phase shift is given by the product of the radian frequency and the time delay, and thus the phase shift is proportional to frequency. However, the system gain would be independent of frequency in a properly balanced and matched system. The scheme we have developed uses a variable delay line where the time delay is selected according to the frequency of the input waveform.

## 3. Nonlinear circuit implementations

Implementation of the ideal as specified above can be achieved with analogue circuitry only through the use of nonlinear elements. Then, of course, the effect on non-sinusoidal signals will be dependent on details of the nonlinearity. In many cases it is required to preserve the

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profile of the waveform, where a 'phase shift' requires the delay of the wavetrain by a certain fraction of the period. It may be that square waves are being used.

Square-wave reference signals are often used for lock-in detection, where they eliminate the dependence of the gain on the reference amplitude, but at the expense of an increased noise bandwidth. In low-frequency NMR systems it is convenient to work with square waves where much of the electronics circuitry then may be implemented in TTL logic. A particular advantage of using square waves is that the four quadrature phases may easily be generated by starting with a master oscillator running at four times the operating frequency. Each output of a divide-by-four counter then provides the four quadratures directly (with a 1:1 mark-space ratio, independent of that of the input).

## 4. A switched delay line implementation

There is presently available a growing variety of miniature delay lines produced in standard dual in-line packages and operating at standard TTL levels. A wide range of delay times is available, and Schottky TTL buffering of inputs and outputs is available. A sequence of delays is possible on one chip, and for us the important development was the possibility of binary-coded delay selection. The Newport† 60A series of digital delay modules is a family of three-bit programmable delay devices. Seven incremental delays are thus available on a chip according to the binary setting on the control lines. Presently devices are available with incremental delays of between 1 and 12 ns.

On its own, a three-bit delay line does not provide an adequate range of delay times. However, by simply cascading a 7 × 1 ns device and a 7 × 8 ns device a total delay of 63 ns is possible in 1 ns steps, selected in binary fashion directly by the six control lines. Even this was not quite suitable for our requirements. Ideally a further device with 64 ns increments could be cascaded, but such a component is not available. It was decided that an eight-bit control line was adequate. This gives a maximum delay of 255 ns, equivalent to a shift of just over 90° at 1 MHz, and an eight-bit line interfaces to other circuitry conveniently.

The time-delay unit with the extra two-bits worth of delay is shown in figure 2. The 7 × 9 ns devices each give a delay of 63 ns whereas the actual requirement is 64 ns. However, this was the closest available, and considering the tolerances on the delay times this is quite acceptable. The circuit for the encoder for the two most significant bits is also shown, implemented from nand gates and achievable with two TTL packages. Alternatively a single PAL (programmable array logic) device could be used.

The device described so far produces delays up to 255 ns in 1 ns steps according to the setting of the eight-bit binary control line. The problem then is how to generate this byte. One possibility is to set it from a computer. This is highly feasible for automated spectrometer systems and we do this for certain applications. But our primary concern here is for a manual device which, according to our ideal, gives a phase shift of a specified angle. Now the time delay $t$ required is related to the phase angle $\phi$ and frequency $f$ by

$$t = \phi/2\pi f.$$

The control byte must therefore be proportional to the required phase angle and inversely proportional to frequency. Although digital division is possible, it was decided that analogue circuitry would be simpler. If a

† Newport Components Ltd, 134 Tanners Drive, Blakelands North, Milton Keynes MK14 5BP, UK.

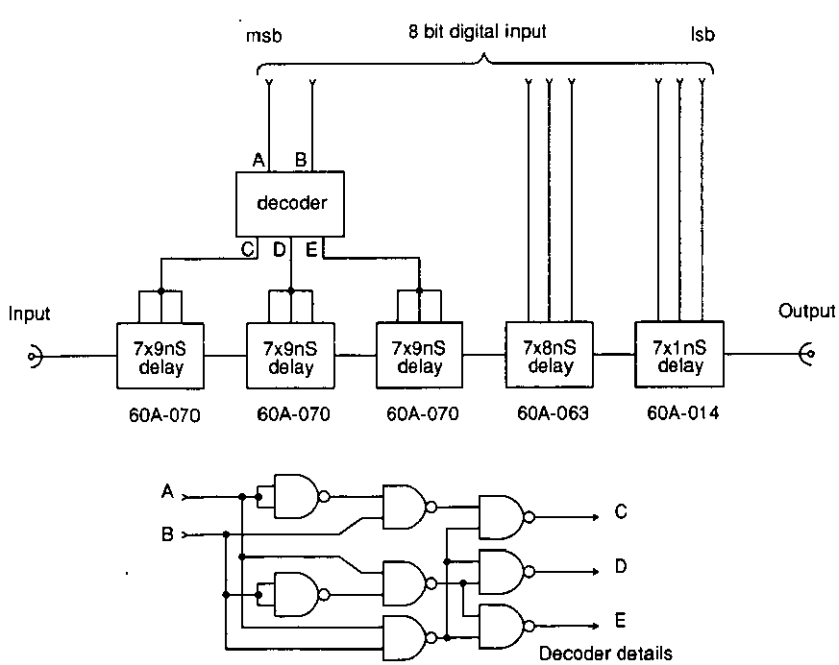


**Figure 2.** Circuit producing time delays up to 255 ns in 1 ns increments.

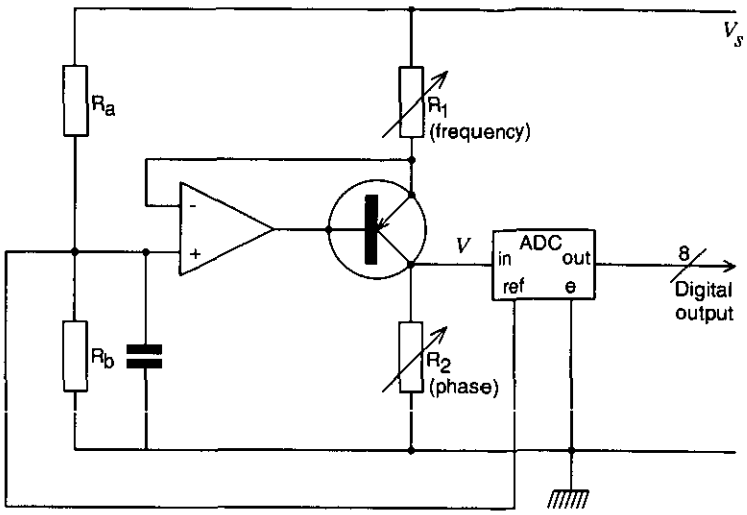


**Figure 3.** Generation of an eight-bit control byte corresponding to a given frequency and phase.

current inversely proportional to frequency can be produced then it can be passed through a resistance proportional to the phase required. The voltage across this resistance then has the required magnitude and can be digitized using an analogue-to-digital converter (ADC). An outline of such a circuit is shown in figure 3.

The non-inverting input of the operational amplifier is maintained at a voltage of $V_sR_a/(R_a+R_b)$ below $V_s$. The feedback then causes the inverting input and hence the voltage across $R_1$ to have the same value. The current flowing through $R_1$ is then

$$I=V_sR_a/(R_a+R_b)R_1.$$

The high gain of the transistor ensures that practically all this current flows out of the emitter, through $R_2$, to earth. The voltage going to the ADC is then

$$V=\{V_sR_a/(R_a+R_b)\}R_2/R_1.$$

It follows that if we set $R_1$ proportional to the frequency and $R_2$ proportional to the phase then the voltage at the ADC will be proportional to the time delay, and so the required binary byte will be produced to send to the delay line assembly.

## 5. Practical performance

Phase shifters built to this design have been in use in our laboratory over the past few months and they have functioned extremely reliably. Resolution is limited by the smallest time increment of the delay line: here 1 ns. This corresponds to a phase angle of 0.36° at 1 MHz and 3.6° at 10 MHz. To eliminate jitter in the least-significant bit we have a hold facility on the ADC that is only released when adjustments are being made. This performance is more than adequate for our requirements. However, if greater resolution is required, we have recently discovered another manufacturer of programmable delay lines, Data Delay Devices†, who manufacture units with a 0.5 ns increment. They also provide eight-bit programmable devices. Thus their use would obviate the need for the decoding circuitry of figure 2.

Our circuit falls short of the ideal in two respects. Firstly it operates with TTL square waves rather than analogue signals of arbitrary profile. This is quite acceptable for us as our mixers and transmitter gates are all TTL driven. If sine waves are required, some form of pulse shaping can be used. The second way in which the ideal is not achieved is that the operating frequency has to be set manually. This is a minor inconvenience and quite acceptable in practice. It is, however, quite possible for a circuit to sense the frequency itself. We are currently developing a system which incorporates this.

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## Reference

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† Data Delay Devices Inc, 3 Mt Prospect Ave., Clifton, New Jersey 07013, USA. (UK agents: BFI IBEXSA Electronics Ltd, BFI IBEXSA House, Burnt Ash Rd, Quarry Wood Estate, Aylesford South ME20 7NA, UK).